Examiner rejected claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over Masayuki (U.S. Patent No. 6,262,488) in view of Chen (U.S. Patent No. 5,761,609) according to the rationale discussed on page 4 of the Office Action. Applicants appreciate the Examiner's early indication of allowable subject matter in this case.

For the following reasons, the rejections are respectfully traversed and reconsideration is respectfully requested.

I. ALLOWABLE SUBJECT MATTER

The Office Action initially states on page 2 that "[c]laims 4 and 24 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. §112, second paragraph, set forth in this Office action...." However, the Office Action does not provide any explicit basis of any rejection of claims 4 and 24 under 35 U.S.C. § 112, second paragraph.

Further, Applicant amends claims 3 and 24 for clarity and to provide antecedent support in view of the Examiner's initial general statement regarding claims 4 and 24 as allowable if remedied to conform with 35 U.S.C. § 112, second paragraph. In claim 3 the word "data" is deleted following the word "identifier" to correspond to the term "identifier" recited in the claim 1, from which claim 3 depends. Applicant asserts that this clarification provides the appropriate antecedent support for the recitation "identifier" in claim 4 which depends from claim 3. Also, in claim 24 the word "resistor" is replaced with the word "resistance" to correspond to the phrase "resistance element" recited in claim 23 from which claim 24 depends. As a result of this Amendment, claims 4 and 24 are in proper condition for Allowance.

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II. REJECTION OF CLAIMS UNDER 35 U.S.C. §102(a)

The Examiner rejected claims 1, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 20, 21, 25, and 26 under 35 U.S.C. § 102(b) as being anticipated by Masayuki (U.S. Patent No. 6,262,488). Applicant points out that although the Office action initially cites U.S. Patent No. 6,262,488 to Masayuki on page 2, the Notice of References Cited lists a different patent to Masayuki: U.S. Patent No. 5,708,298. The Examiner's remarks in the Office Action appear to correspond to either of the above-mentioned patents to Masayuki. As both references appear to have certain similarities, Applicant respectfully requests that the Examiner clarify which (if not both) of the patents to Masayuki (U.S. Patent No. 5,708,298 and/or U.S. Patent No. 7,262,488) have been applied by the Examiner and to reflect the same in Form PTO-897 so that the written record win this case will be complete.

Further, in the Office Action the Examiner asserts that Masayuki anticipates claims 1, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 20, 21, 25, and 26 under 35 U.S.C. 102(b). However, because Masayuki fails to disclose each and every element recited in the claims, Applicant respectfully traverses this ground of rejection.

Independent claims 1, 10, 15, and 25 patentably distinguish the present invention from the teachings of Masayuki. For example, independent claim 1 recites a combination of elements that includes, among other things,

> an identifying unit which includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal, and an identifier generating

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circuit for generating identifiers for other memory units on the basis of the identifier,

(independent claim 1, lines 5-11). At the very least, Masayuki does not disclose these exemplary features.

To anticipate independent claim 1 under 35 U.S.C. § 102(a), Masayuki, taken individually, must explicitly disclose each and every element recited in the claim either expressly or inherently. *See* M.P.E.P. § 2131.

Masayuki discloses a semiconductor device with a module base plate 1 which is "constructed by stacking pluralities of ceramic layers and wiring layers by the use of laminated ceramic." *See* col. 5, lines 37-40. This is accomplished by stacking eight semiconductor chips on each of the front surface and rear surface of the module base plate 1. *See* col. 5, lines 40-42. Each semiconductor chip includes a static RAM and bump electrodes 6 to which various leads 5A, 5B, 5C, and 5D are respectively connected. *See* col. 5, lines 47-50. The individual leads 5B are connected to a decoder 3 and leads 2 through wiring. *See* col. 5, lines 64-66. Finally, the lead 5A, for inputting a chip select signal to the semiconductor chip 4A is connected to the lead 3A of the decoder 3 without being connected with the lead 5B for inputting a chip select signal to the semiconductor chip 4B. *See* col. 5, line 66 - col. 6, line 3. Accordingly, Masayuki is directed to a technique for stacking memory chips.

By contrast, claim 1 recites a semiconductor device that includes, among other things, "an identifying unit which includes ... a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal, and an identifier generating circuit for generating

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identifiers for other memory units on the basis of the identifier." Masayuki does not disclose at least these features.

Furthermore, independent claim 10 recites, in part,

> an identifying unit which is provided outside the memory unit and includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned thereto and a memory unit selecting signal, and an identifier generating circuit or generating identifiers for other memory units on the bass of the identifier of the memory unit,

(independent claim 10, lines 13-17). As Masayuki does not disclose at least these features of claim 10, it fails to anticipate that claim.

Next, independent claim 15 is directed to a semiconductor module including, among other things,

> a first identifying unit including at least: a first memory unit selecting circuit for selecting the first memory unit on the basis of a first identifier assigned thereto and the memory unit selection signal; and a first identifier generating circuit for generating a second identifier for the second memory unit on the basis of the first identifier; and
>
> a second identifying unit including at least: a second memory unit selecting circuit for selecting the second memory unit on the basis of the second identifier assigned thereto and the memory unit selection signal; and a second identifier generating circuit for generating a third identifier for a third memory unit on the basis of the second identifier,

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(independent claim 15, lines 6-15). As discussed above, Masayuki is directed to a stacking method for semiconductor chips. Masayuki does not disclose at least these features of claim 15.

Finally, independent claim 25 includes, among other things,

> an identifying unit at least including an identifier generating circuit provided with at least a wire for generating an identifier for the memory unit, and a memory unit selecting circuit for selecting the memory unit on the basis of the identifier assigned thereto and the memory unit selecting signal,

(independent claim 25, lines 30-33). Masayuki does not disclose at least these features of independent claim 25.

For at least the above reasons, Masayuki does not disclose each and every element recited in independent claims 1, 10, 15, and 25. Moreover, claims 3-5, 7, 9-14, 17, 19-21, and 26, which each depends upon one of the independent claims, respectively, recite additional features that are neither disclosed by Masayuki. Thus, claims 3-5, 7, 9-14, 17, 19-21, and 26, are allowable for at least the same reasons as discussed above with respect to allowable independent claims 1, 10, 15, and 25.

III. REJECTION OF CLAIMS UNDER 35 U.S.C. § 103(a)

Claims 2, 3, 6, 8, 16, and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki (U.S. Patent No. 6,262,488) in view of Kasa (U.S. Patent No. 5,179,536) according to the rationale given on pages 3-4 of the Office Action. The Examiner alleges on page 4 of the Office Action that "Masayuki et al. show all the claimed subject matter in 2, 3, 6, 8, 16, and 18, except that they fail to describe an adder circuit adder and comparator and they also fail to include a ROM, EPROM, or

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EEPROM. However, in Fig. 39 of Masayuki, item 532 is an adder and item 522 is a comparator." Applicant respectfully points out that Fig. 39 in Masayuki does not contain elements numbered as described in the Office Action. From the information provided in the Office Action, it appears that Kasa may be the reference that the Examiner is referring to in the above-quoted excerpt. Assuming that to be the case, this ground of rejection is respectfully traversed for the following reasons.

As discussed above, Masayuki does not disclose each and every element recited in independent claims 1 and 15. Furthermore, Kasa fails to make up for the deficiencies of Masayuki. For example, independent claim 1 recites a combination of elements that includes, *inter alia*, "an identifying unit which includes at least a memory unit selecting circuit for selecting the memory unit on the basis of an identifier assigned to the memory unit and the memory unit selecting signal; and an identifier generating circuit for generating identifiers for other memory units on the basis of the identifier." Independent claim 15 recites a combination of elements that includes, *inter alia*, "a first identifying unit including at least: a first memory unit selecting circuit for selecting the first memory unit on the basis of a first identifier assigned thereto and the memory unit selection signal; and a first identifier generating circuit for generating a second identifier for the second memory unit on the basis of the first identifier; and a second identifying unit including at least: a second memory unit selecting circuit for selecting the second memory unit on the basis of the second identifier assigned thereto and the memory unit selection signal; and a second identifier generating circuit for generating a third identifier for a third memory unit on the basis of the second identifier." Neither Masayuki nor Kasa taken alone or in combination teaches or suggests at least these elements. As

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claims 2, 3, 6, 8, 16, and 18 each depend from independent claims 1 and 15, for at least this reason, the combination of Masayuki and Kasa fails to disclose or suggest each and every element recited in claims 2, 3, 6, 8, 16, and 18.

Moreover, to establish a *prima facie* case of obviousness under 35 U.S.C. § 103, each of three requirements must be demonstrated. First, Masayuki and Kasa, when combined as a whole, must disclose or suggest each and every element recited in the claims. *See* M.P.E.P. § 2143.03. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. *See id.* Third, a reasonable probability of success must exist. *See id.* Furthermore, each of the these requirements must "be found in the prior art, and not based on applicant's disclosure." *See* M.P.E.P. § 2143.

Kasa is directed to a semiconductor memory device comprising memory cells for pre-storing fixed data and for replacing defective memory cells. For example, Kasa states that the "defective memory cell within the mask ROM cell array 16 is substituted by the PROM cell array 23 and the defective memory cells are relieved." *See* col. 5, lines 41-44. Kasa fails to make up for the deficiencies of Masayuki. Applicant respectfully submits that the Examiner has not shown that the combination of Masayuki and Kasa would provide the artisan or one of ordinary skill with a suggestion or motivation, at the time of making the invention, to combine the references so that it would include all of the elements recited in claims 2, 3, 6, 8, 16, and 18.

Claim 2 recites a combination of elements, including, *inter alia*, "wherein the identifier generating circuit is mainly constituted by an adder circuit or a subtractor

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circuit." Claim 3 recites a combination of elements, including, *inter alia*, "wherein the identifier is one bit data or a plurality of bit data, and the identifier generating circuit is an adder circuit for carrying the identifier data of the memory unit bit by bit." Claim 6 recites a combination of elements, including, *inter alia*, "wherein the memory unit selecting circuit is a comparator for compares the identifier with the memory unit selecting signal." Claim 8 recites a combination of elements, including, *inter alia*, "wherein the memory unit is a non-volatile memory which is ROM, EPROM or EEPROM." Claim 16 recites a combination of elements including, *inter alia*, "wherein the first and second identifier generating circuits are mainly constituted by adder or subtractor circuits." Claim 18 recites a combination of elements, including, *inter alia*, "wherein the first memory unit selecting circuit is a comparator for comparing the first identifier and the memory unit selecting signal, and the second memory unit selecting circuit is a comparator for comparing the second identifier and the memory unit selecting signal."

A statement by the Examiner that "[i]t would have been obvious to one of having ordinary skill in the art to include an adder circuitry, a comparator in decoder and associated circuitry in an programmable memory [of] Masayuki et al. as taught by Kasa et al. because such structure would provide a better flexibility" does not meet the burden of showing the necessary motivation to make the proposed combination and is insufficient to support the rejection. (Office Action, page 4). The Examiner has made an allegation without any factual evidence, such as a citation to a competent reference. Moreover, Kasa is directed to a semiconductor memory device comprising memory cells for pre-storing fixed data and for replacing defective memory cells. No motivation exists

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for combing the teachings of Kasa with the stacking method for semiconductor chips disclosed in Masayuki. In the absence of a factual basis that would demonstrate the suggestion or motivation to combine the references in a manner resulting in the claimed invention, a *prima facie* case of obviousness has not been made and the rejection should be withdrawn.

For at least the above reasons, Masayuki and Kasa fail to suggest or motivate each and every element recited in claims 2, 3, 6, 8, 16, and 18. Moreover, claims 2, 3, 6, 8, 16, and 18, which each depends upon one of the independent claims, respectively, recite additional features that are neither disclosed nor suggested by any of the cited references, taken either alone or in combination. Accordingly, claims 2, 3, 6, 8, 16, and 18 are allowable for at least the same reasons discussed above with respect to allowable independent claims 1 and 15. For at least these reasons, Applicant respectfully requests that the Examiner withdraw the rejection and allow claims 2, 3, 6, 8, 16, and 18.

Additionally, claims 22 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki (U.S. Patent No. 6,262,488) in view of Chen (U.S. Patent No. 5,761,609). Chen discloses a limited use circuit that may be used only a limited number of times so that copying or unauthorized use of an electronic system may be prevented. *See* col. 2, lines 36-40.

Masayuki does not disclose each and every element recited in independent claim 22. Furthermore, Chen fails to make up for the deficiencies of Masayuki. For example, independent claim 22 recites, in part, "an identifying unit at least including an identifier generating circuit provided with at least a fuse element for generating an identifier

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assigned to the memory unit" (independent claim 22, lines 9-12). Neither Masayuki nor Chen taken alone or in combination teaches or suggests at least these elements. As claim 23 depends from independent claim 22, for at least this reason, the combination of Masayuki and Chen fails to disclose or suggest each and every element recited in claims 22 and 23.

Moreover, the combination of Masayuki and Chen does not motivate or suggest each and every element recited in claims 22 and 23. Independent claim 22 recites, in part, "an identifying unit at least including an identifier generating circuit provided with at least a fuse element for generating an identifier assigned to the memory unit." Claim 23 recites, in part, a combination "wherein the identifier generating circuit further includes a resistance element." The combination of Masayuki and Chen does not motivate or suggest at least these features of the present invention.

The Examiner states that "it would have been obvious to one of having ordinary skill in the art to include a fuse and resistor structure to the semiconductor module of Masayuki et al. as taught by Chen because such structure would provide a better programmability." (Office Action, page 4). Chen solely discloses a limited use circuit that may be used only a limited number of times. A fuse burning device 20 receives signals 22 from the mask circuit 18 of the state machine. *See* col. 4, lines 2-3. Nothing in Chen motivates or discloses a combination including "an identifying unit at least including an identifier generating circuit provided with at least a fuse element for generating an identifier assigned to the memory unit," as recited in claim 22.

Moreover, Chen discusses the use of a resistor 26 that acts as a fuse state indicator such that the state of the fuse 26 may be read from signal 28. *See* col. 4,

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lines 9-11. Chen does not motivate or disclose at least a combination "wherein the identifier generating circuit further includes a resistance element," as recited in claim 23. The Examiner's allegation without any factual evidence, such as a citation to a competent reference, does not meet the burden of showing the necessary motivation to make the proposed combination and is insufficient to support the rejection.

For at least these reasons, Masayuki and Chen fail to motivate or suggest each and every element recited in claims 22 and 23. Moreover, claims 22 and 23 recite additional features that are neither disclosed nor suggested by any of the cited references, taken either alone or in combination. Applicant respectfully requests that the Examiner withdraw the rejection and allow claims 22 and 23.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-26 define patentable subject matter and that the application is in condition for allowance. Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: September, 23, 2002

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APPENDIX TO AMENDMENT DATED SEPTEMBER 23, 2002

AMENDMENTS TO THE CLAIMS:

3. (AMENDED) The semiconductor device of claim 2, wherein the identifier is one bit data or a plurality of bit data, and the identifier generating circuit is an adder circuit for carrying the identifier [data] of the memory unit bit by bit.

6. (AMENDED) The semiconductor device of claim 1, wherein the memory unit selecting circuit is a comparator for [compares] comparing the identifier with the memory unit selecting signal.

18. (AMENDED) The semiconductor module of claim 15, wherein the first memory unit selecting circuit is a comparator for [compares] comparing the first identifier and the memory unit selecting signal, and the second memory unit selecting circuit is a comparator for [compares] comparing the second identifier and the memory unit selecting signal.

24. (AMENDED) The semiconductor device of claim 23, wherein the [resistor] resistance element has a resistance value which is higher than a resistance value of the fuse element.

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